

EXHIBIT 3



US007225282B1

(12) **United States Patent**
Lyle

(10) **Patent No.:** **US 7,225,282 B1**
(45) **Date of Patent:** **May 29, 2007**

(54) **METHOD AND APPARATUS FOR A TWO-WIRE SERIAL COMMAND BUS INTERFACE**

(75) Inventor: **Jim Lyle**, Santa Clara, CA (US)

(73) Assignee: **Silicon Image, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1012 days.

(21) Appl. No.: **10/171,820**

(22) Filed: **Jun. 13, 2002**

(51) **Int. Cl.**
G06F 13/42 (2006.01)

(52) **U.S. Cl.** **710/105; 710/306**

(58) **Field of Classification Search** **710/100, 710/105, 306, 310; 370/401**

See application file for complete search history.

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Primary Examiner—Rehana Perveen

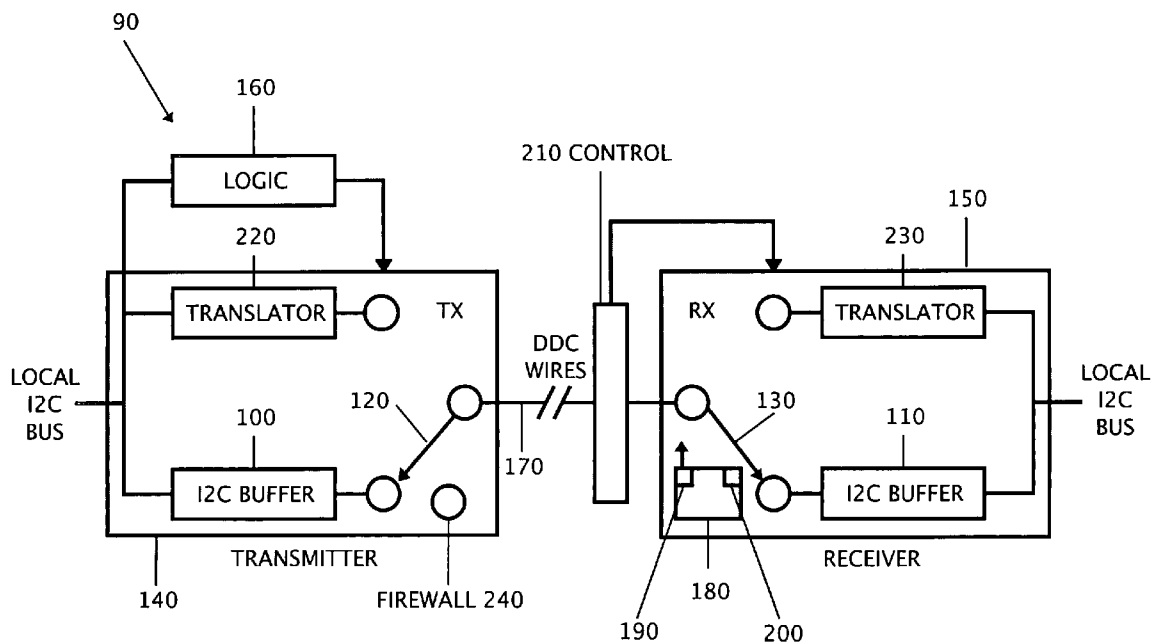
Assistant Examiner—Clifford Knoll

(74) *Attorney, Agent, or Firm*—Perkins Coie LLP

(57) **ABSTRACT**

A method for bi-directional transmission of data between a source and a sink over a two-wire interface includes re-mapping a data signal and a clock signal from a first local bus on the source into a different protocol signal. Transmitting the different protocol signal from the source to the sink over the two-wire interface. Re-mapping the different protocol signal back into the data signal and the clock signal for use on a second local bus on the sink. Re-mapping the data signal and the clock signal from the second local bus into the different protocol signal; and transmitting the different protocol signal from the sink to the source over the two-wire interface.

37 Claims, 10 Drawing Sheets



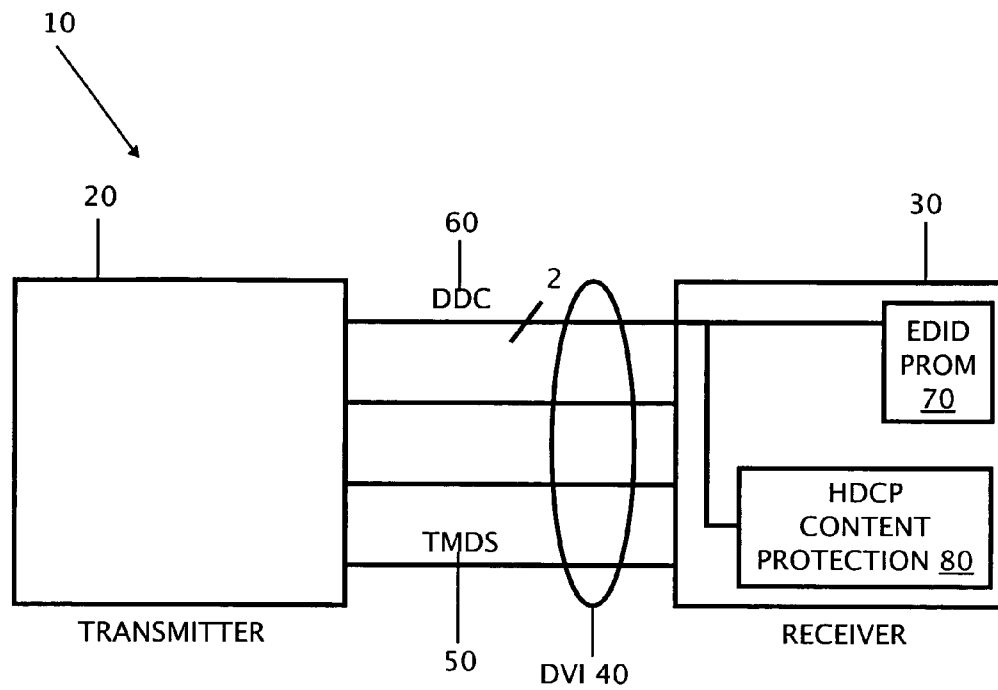


FIG. 1
(PRIOR ART)

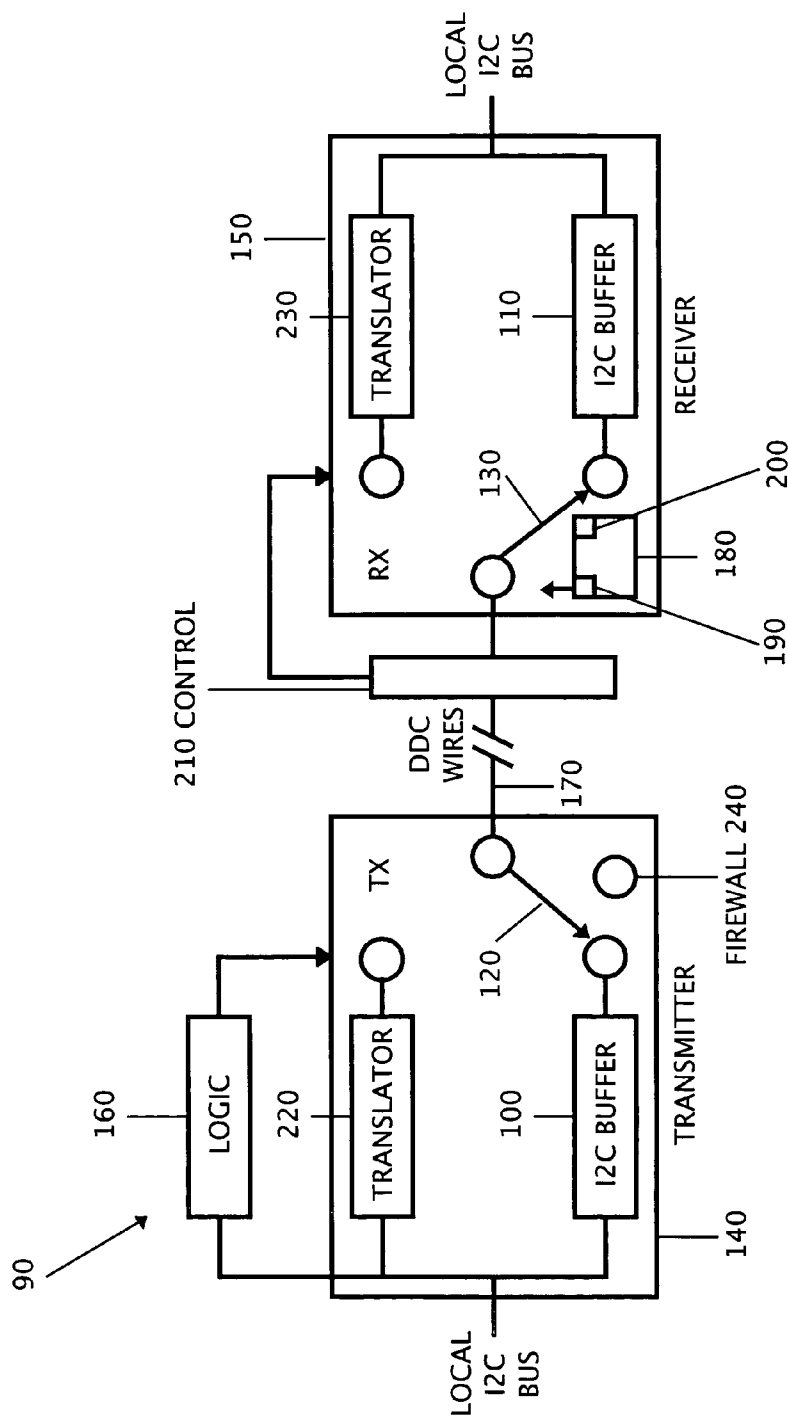


FIG. 2A

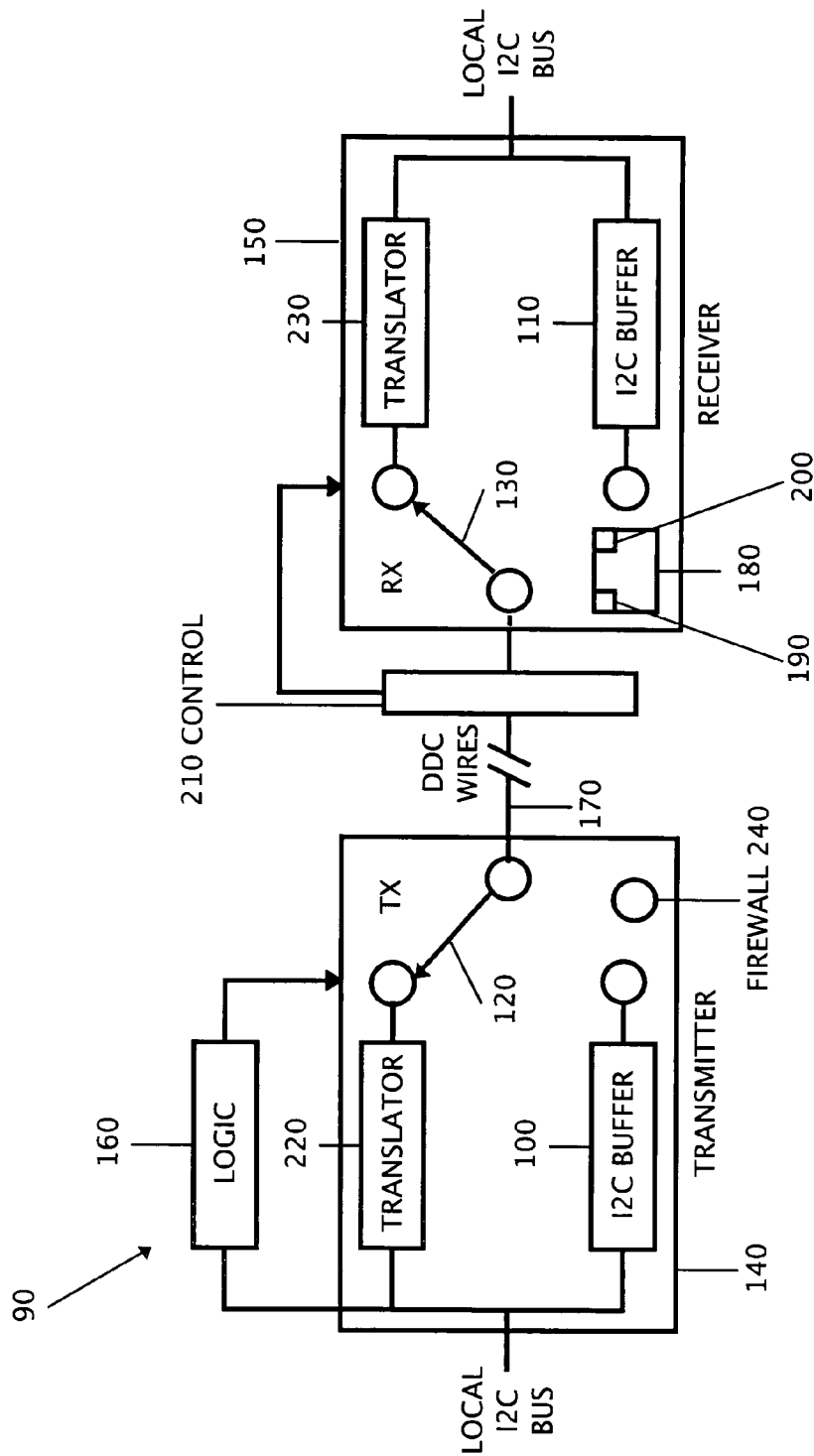


FIG. 2B

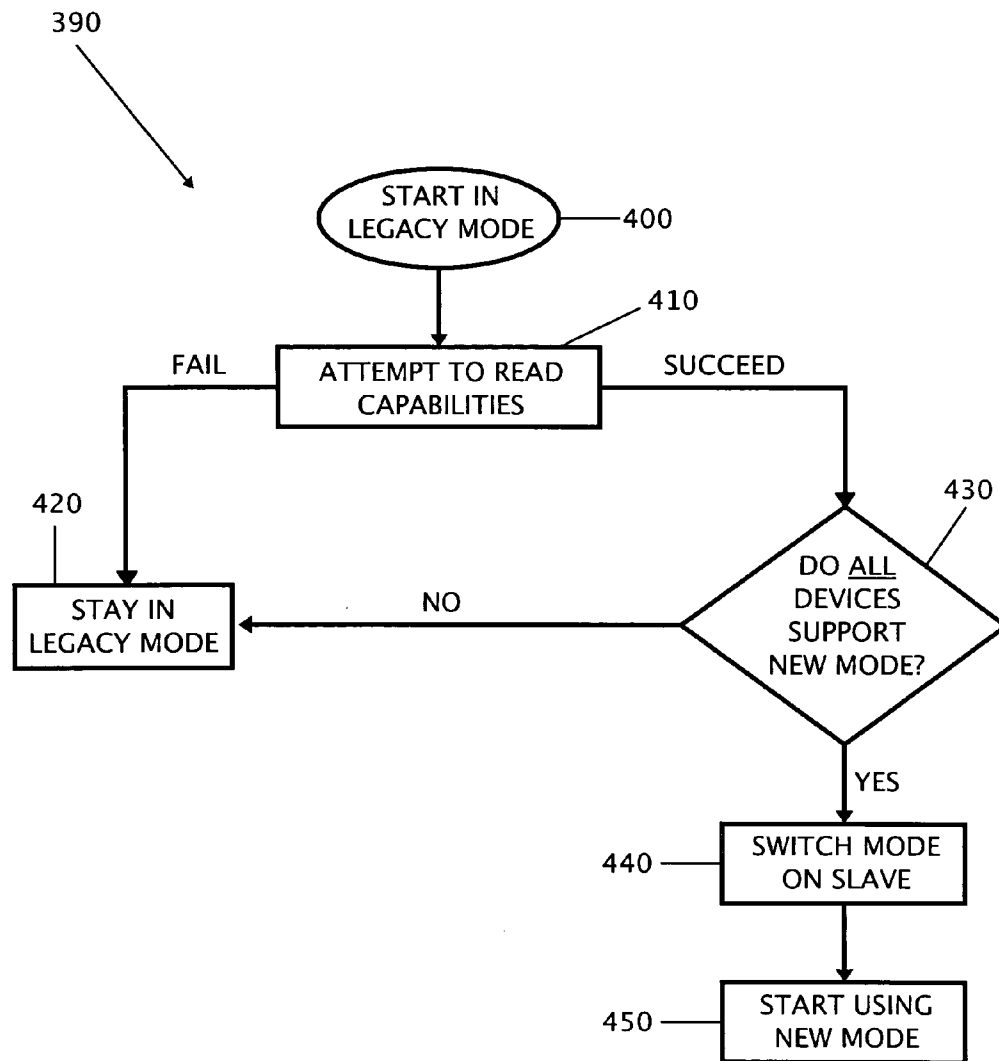


FIG. 3A
"NEGOTIATE AND SET"

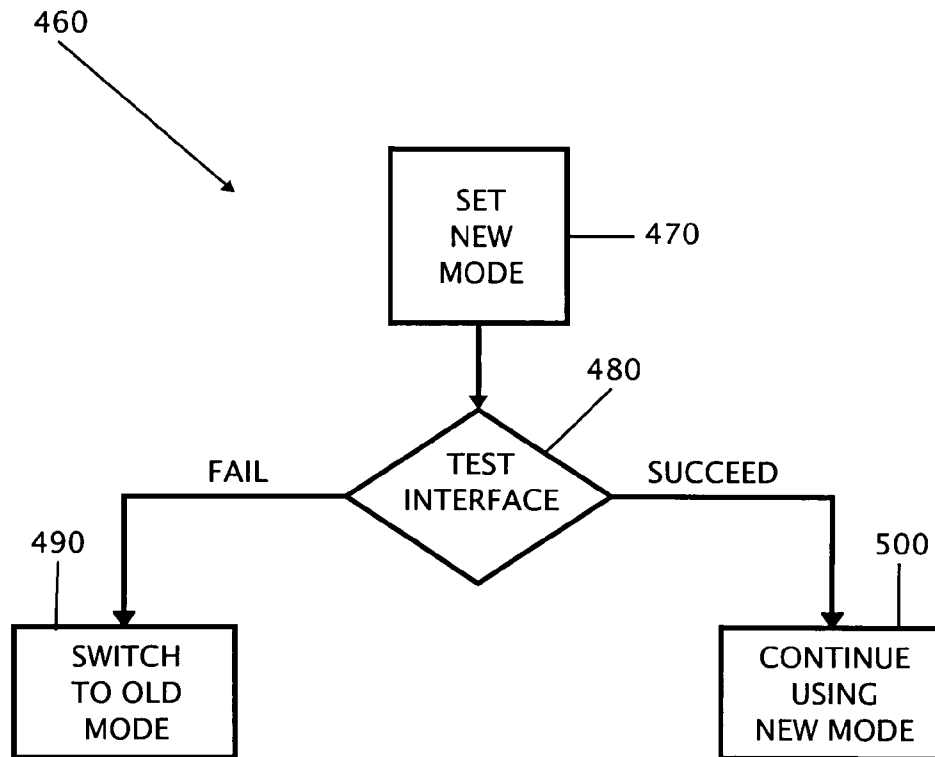


FIG. 3B
"SET AND TEST"

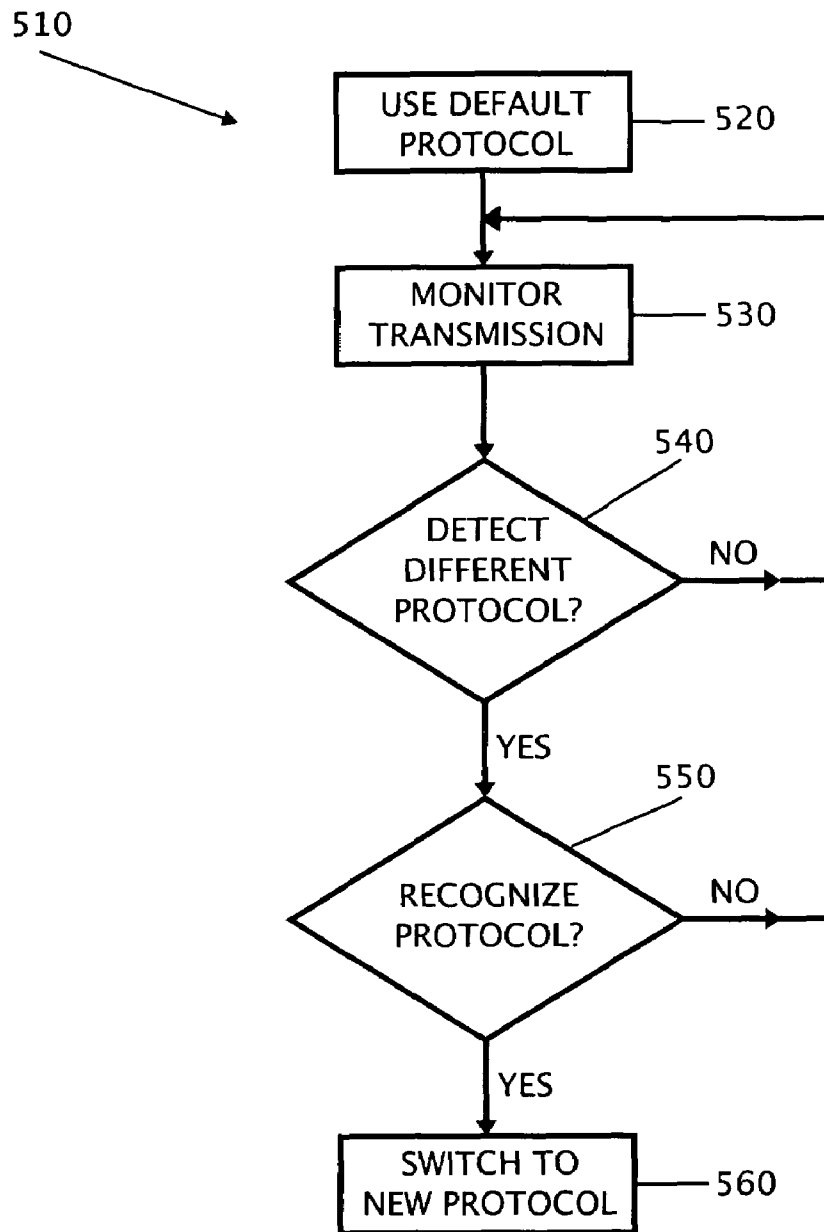


FIG. 3C

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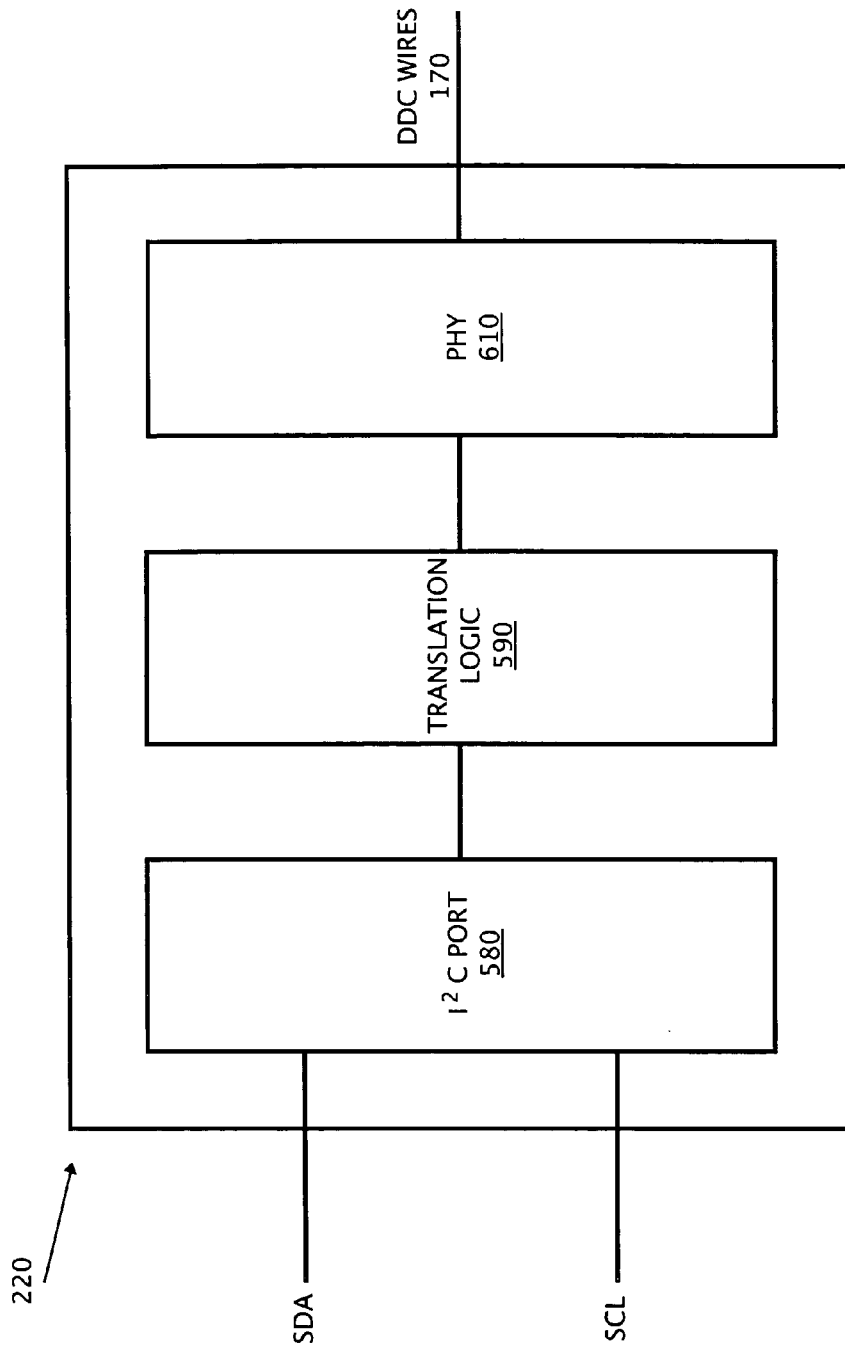


FIG. 4

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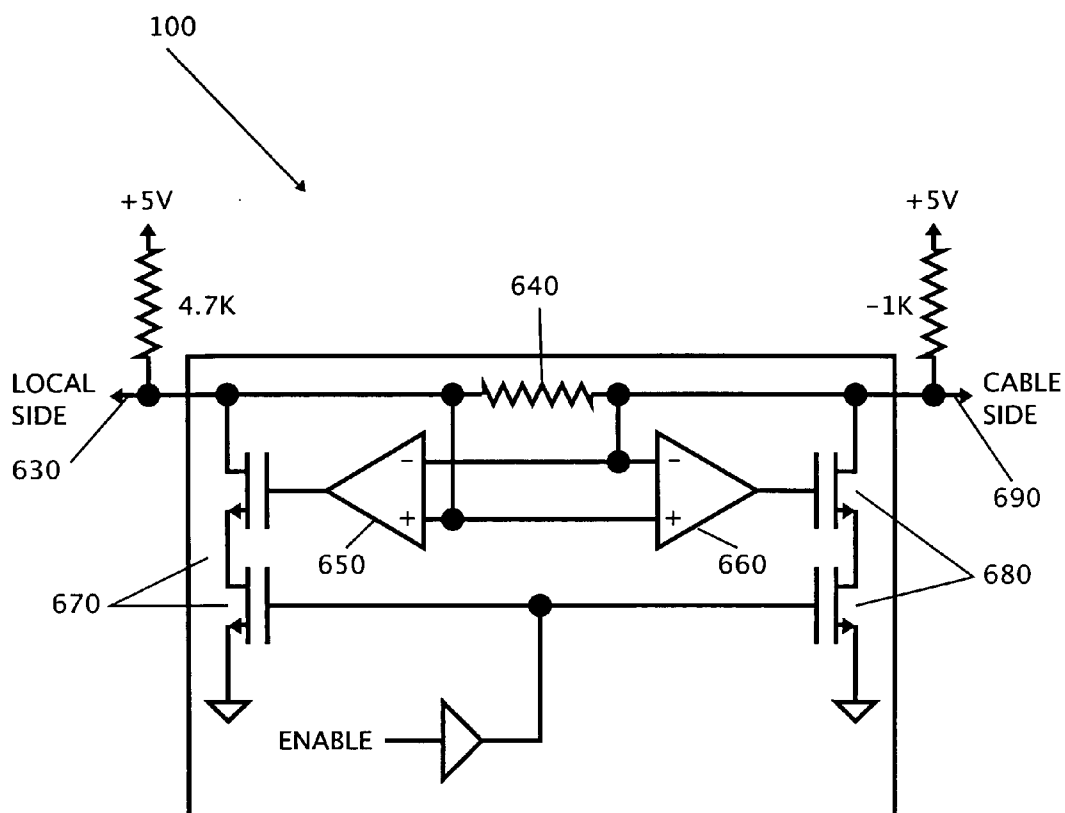


FIG. 5

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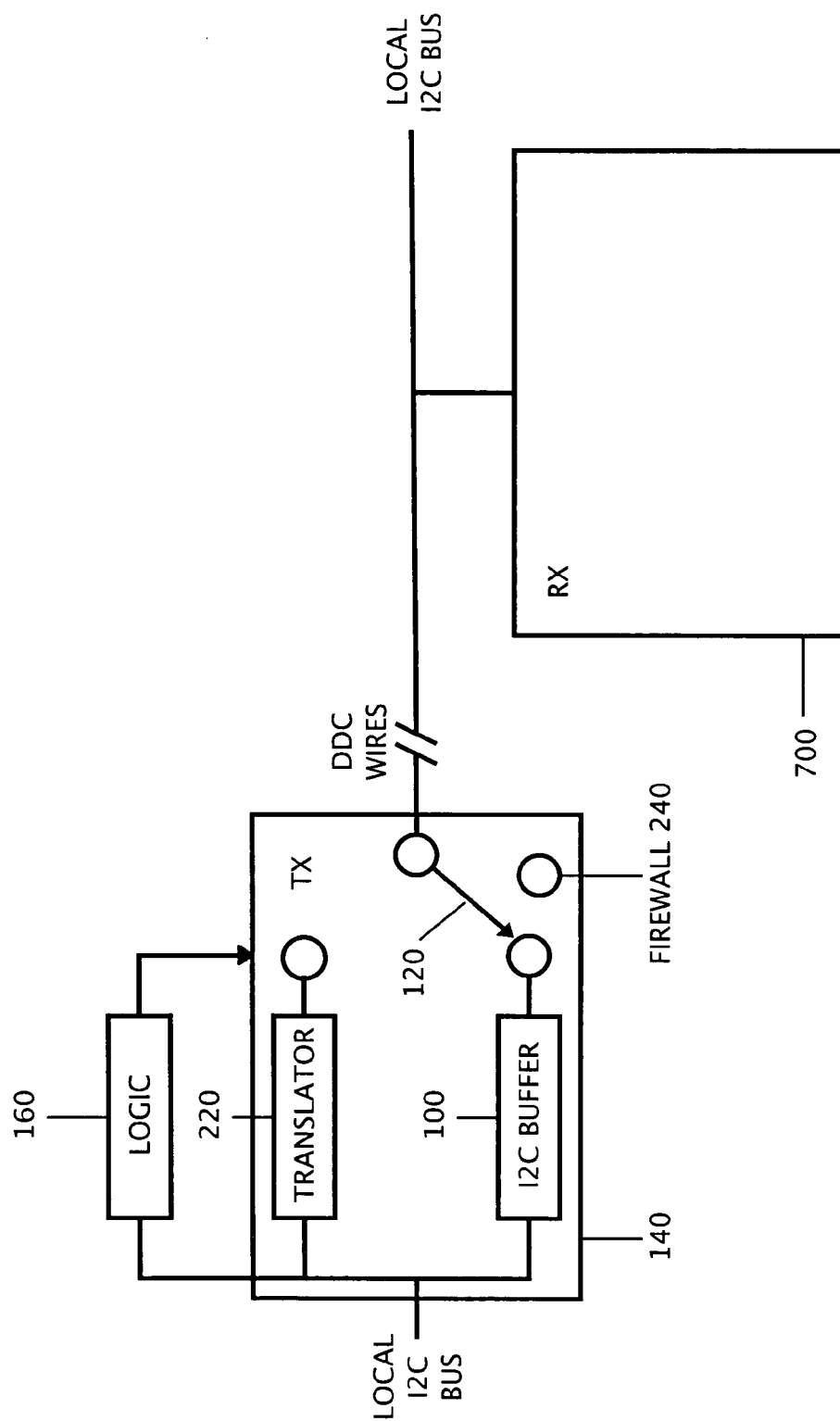


FIG. 6

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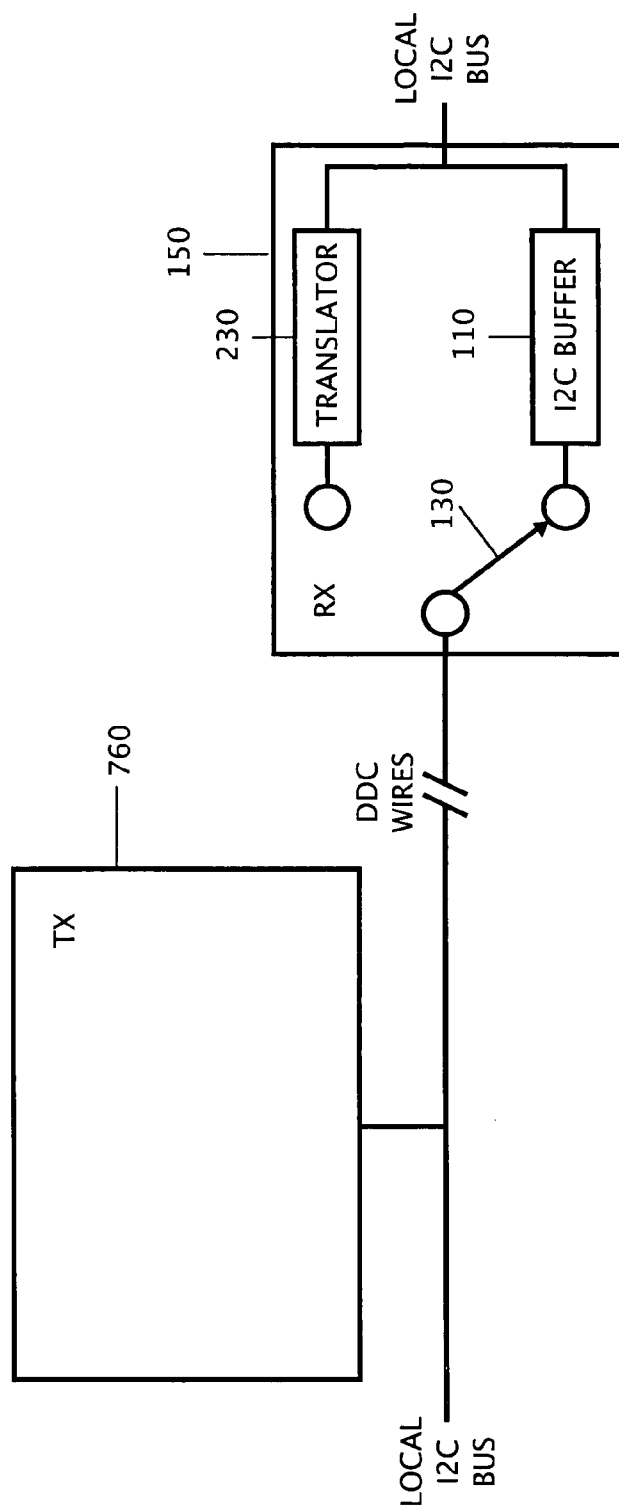


FIG. 7

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METHOD AND APPARATUS FOR A TWO-WIRE SERIAL COMMAND BUS INTERFACE

FIELD OF THE INVENTION

The present invention relates generally to digital communication between a transmitter and a receiver, and more particularly to communication between a video source device and a video display device.

BACKGROUND OF THE INVENTION

FIG. 1 illustrates a prior art system 10 of how a transmitter 20 and a receiver 30 communicate. The transmitter 20 can be, for example, a computer, a DVD player or other video source and the receiver 30 can be a monitor or a television. Communication between the transmitter 20 and the receiver 30 is typically achieved via the DVI (digital visual interface) 40 which is a single interface that contains various lines bundled into one cable. An HDMI link (high definition multi-media interface) or some other variant can also achieve communication between the transmitter 20 and the receiver 30. Some of these lines include a hot plug signal, a power line, TMDS® (transition minimized differential signaling) 50 (typically used for carrying video data) and a DDC (display data channel) bus 60.

The DDC bus 60 is a serial 2-wire interface that has one data line and one clock line. This serial protocol is believed to have been developed, at least in part by the Philips Corporation of Holland. Philips part #PCA9515 is an integrated circuit which implements the so-called I²C bus. One of the primary purposes of the DDC bus 60, when used as an I²C bus, is to read an EDID PROM 70 (extended data interface device programmable read only memory) which includes data concerning the receiver 30. The DDC bus 60 can also be used for data transfer with HDCP 80 (high-bandwidth digital content protection), which is an encryption device that provides content protection.

Several problems are associated with the DDC bus 60 that make it undesirable for certain applications. One problem is that it can not be of an extended physical length due to electrical issues such as overwhelmed capacitive load budgets and transmission line effects that degrade signal timing parameters. Another problem is that its data carrying capacity is limited to about 400 kilobits/second. The data on the DDC bus 60 can be easily eavesdropped and even manipulated and since it may connect to several devices in the transmitter 20, security is also an issue. Finally, any attempt to solve these problems would need to take into consideration legacy issues for the purpose of backward compatibility. That is, the DDC bus is very widely used and any attempt to improve upon it would need to be compatible with transmitters and receivers that use the standard DDC bus interface.

Accordingly, what is needed is a method and apparatus for a DDC compatible two-wire serial command interface which allows for high speed data transmission, extended cable length, data security and still provide backward compatibility.

SUMMARY OF THE INVENTION

The present invention provides a system and method for intelligently re-mapping a two-wire interface between a transmitter and a receiver. The re-mapping allows for high speed data transmission and data security and is not con-

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strained by length issues. Additionally, a transmitter-side firewall prevents unauthorized access.

A method for bi-directional transmission of data between a source and a sink over a two-wire interface, in accordance with the present invention, includes re-mapping a data signal and a clock signal from a first local bus on the source into a different protocol signal. Transmitting the different protocol signal from the source to the sink over the two-wire interface. Re-mapping the different protocol signal back into the data signal and the clock signal for use on a second local bus on the sink. Re-mapping the data signal and the clock signal from the second local bus into the different protocol signal; and transmitting the different protocol signal from the sink to the source over the two-wire interface.

A system for bi-directional transmission of data between a source and sink over a two-wire interface, in accordance with the present invention, includes a first translator that is responsive to and operative to develop a first local bus signal and is responsive to and operative to develop a different protocol signal. A first buffer is responsive to and operative to develop the first local bus signal and is responsive to and operative to develop a buffered data signal and a buffered clock signal. Logic is responsive to the first local bus signal and operative to controlling a first switch coupled to the two-wire interface wherein the switch connects to the first translator, the first buffer or a firewall setting. A second translator is responsive to and operative to develop the different protocol signal and is responsive to and operative to develop a second local bus signal when the first switch is connected to the first translator and a second switch coupled to the two-wire interface is connected to the second translator. A second buffer is responsive to and operative to develop the buffered data signal and the buffered clock signal and is responsive to and operative to develop the second local bus signal when the first switch is connected to the first buffer and the second switch coupled to the two-wire interface is connected to the second buffer.

A method for buffering data between a source and a sink over a two-wire interface, in accordance with yet another aspect of the present invention, includes buffering on the source a data signal and a clock signal received from a local bus on the source. Transmitting, from the source to the sink, the data and clock signals over the two-wire interface. Buffering at the sink the data and clock signals. Re-transmitting from the sink the data and clock signals over the two-wire interface to the source as needed; and logic on the source that performs a firewall function by selectively closing access to the two-wire interface.

A system for buffering data between a source and a sink over a two-wire interface, in accordance with the present invention, includes a first buffer responsive to a first local bus signal and responsive to and operative to develop a buffered data signal and a buffered clock signal. A logic is responsive to the first local bus signal and operative to controlling a first switch coupled to the two-wire interface wherein the switch connects to the first buffer or a firewall setting. A second buffer is responsive to and operative to develop the buffered data signal and the buffered clock signal and is responsive to and operative to develop a second local bus signal when the first switch is connected to the first buffer and a second switch coupled to the two-wire interface is connected to the second buffer.

A system for buffering data between a source and a sink over a two-wire interface, in accordance with the present invention, includes a first buffer that is responsive to a first local bus signal and operative to develop a buffered data signal and a buffered clock signal. A logic is responsive to

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the first local bus and operative to controlling a first switch coupled to the two-wire interface wherein the switch connects to the first buffer or a firewall setting. The sink is coupled to the two-wire interface and is responsive to the buffered data signal and the buffered clock signal when the switch is connected to the first buffer.

An advantage of the present invention is that it is fully compatible with legacy hardware. It intelligently detects whether a device can support new or old protocols and adjusts accordingly. Additionally, even in the absence of new protocol compatibility, it improves upon legacy systems by increasing available cable length and also by providing a transmitter-side firewall. Also, security is improved and new protocols can be designed to be more readily sent through a receiver to another device or another level, for example, though a repeater coupled to two receivers.

These and other advantages of the present invention will become apparent to those skilled in the art after reading the following descriptions and studying the various figures of the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a prior art system of how a transmitter and a receiver communicate.

FIG. 2A illustrates a transmitter and receiver communication system via buffers in accordance with the present invention.

FIG. 2B illustrates a transmitter and receiver communication system via translators in accordance with the present invention.

FIG. 3A illustrates a flow diagram for a “negotiate and set” process in accordance with the present invention.

FIG. 3B illustrates a flow diagram for a “set and test” process in accordance with the present invention.

FIG. 3C illustrates a flow diagram for a “snoop and test” process in accordance with the present invention.

FIG. 4 illustrates a translator in accordance with the present invention.

FIG. 5 illustrates a general implementation of a buffer for an I²C bus in accordance with the present invention.

FIG. 6 illustrates a legacy mode of operation in relation to the receiver in accordance with the present invention.

FIG. 7 illustrates a legacy mode of operation in relation to the transmitter in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 was described with reference to the prior art. FIG. 2A illustrates a transmitter and receiver communication system 90 via buffers 100 and 110 in accordance with the present invention. In the context of the present invention, it should be understood that the terms “transmitter”, “host” and “source” can be used interchangeably and refers to devices capable of sending out signals that can control some other device as well as receive signals from that device. Also, it should be understood that “slave”, “receiver” and “sink” can also be used interchangeably and refers to a device that is controlled by a transmitter via signals and can send out signals to the transmitter.

FIG. 2A depicts a default mode in that, at system startup, switches 120 and 130 are connected to I²C buses 100 and 110, located on transmitter 140 and receiver 150 respectively. Other default modes are also available. Logic 160 sends a signal over DDC wires 170 and reads register 180. Contained within register 180, there is a control bit 190 and

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a status bit 200 that contain information on what the receiver 150 is capable of. Depending on that information, logic 160 will direct control 210 to keep switches 120 and 130 in their default positions or switch to translators 220 and 230. This is one example of how the proper mode to use is determined. This example and others will be fully explained subsequently.

If switches 120 and 130 are left in their default modes, improvements are still evident over prior art systems due to the presence of the buffers 100 and 110 and firewall setting 240. By buffering, the length of the DDC wires can be extended. On the transmitter 140, switch 120 can be placed at firewall setting 240 by logic 160. When firewall setting 240 is selected, access to the transmitter 140 via DDC wires 170 is cut off. Advantageously, this provides greater security on the transmitter 140 since access via the DDC wires 170 can be controlled and is no longer in a perpetually connected state. Additionally, in the context of the present invention, it should be understood that the terms “protocol” and “mode” can be used interchangeably and refer to a specified format of data communication or data transfer.

FIG. 2B illustrates a transmitter and receiver communication system 90 via translators 220 and 230 in accordance with the present invention. Switches 120 and 130, located on transmitter 140 and receiver 150 respectively, are connected to translators 220 and 230. In this particular example, logic 160 directed control 210 to connect switches 120 and 130 to translators 220 and 230 due to information contained in register 180. Specifically, control bit 190 and status bit 200 indicated that the receiver is capable of using the new protocol. This is one example of how the proper mode to use is determined, and this and other examples will be more fully explained subsequently. When the new protocol can be employed, more efficient signaling can be used to improve transmission speed, extend wire length and improve security by encryption. Some example signaling techniques include well-known TCP/IP, differential signaling, ethernet and current loop. Any of these signaling techniques can additionally be encrypted. Translator 220 converts the I²C signal into the new protocol and transmits it over DDC wires 170. Translator 230 then converts the new protocol back into an I²C signal for use on the receiver 150. Since the pre-existing DDC wires 170 are used to transmit the old as well as new protocols, compatibility with legacy hardware is achieved. Additionally, a firewall setting 240 is available on transmitter 140 and operates in the same manner as firewall setting 240 of FIG. 2A.

It should be understood that the receiver 150 could also send information to the transmitter 140. It will also be appreciated that, in some circumstances, the receiver 150 can initiate communications with the transmitter.

In an additional embodiment, both default and new modes (as shown in FIGS. 2A and 2B) can be used simultaneously in a manner that is similar in concept to DSL (digital subscriber line). In DSL, a high speed Internet connection is transmitted on the same wire or sets of wires as an old-style telephone signal by separating the two signals in the frequency spectrum. The same technique can be used for the present invention. The switch 120, in this case, would act as a mixer and blend the two signals for transmission on the DDC wires 170. Switch 130 would then act as a separator and on the receiving side. Besides a frequency spectrum separation of the signals, a voltage separating technique could also be used.

FIG. 3A illustrates a flow diagram for a “negotiate and set” process 390 in accordance with the present invention. The negotiate and set process 390 is one example of how

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logic 160 and logic 320 function. In an operation 400, the legacy mode or old style of communication over a set of DDC wires is used. At operation 410, the capabilities of the receiver (for example receivers 150 or 310) are determined. This is accomplished by reading bit registers 180 and 340 or by reading an EDID PROM 70. It can also be accomplished if the operation fails which is an indication that the receiver does not have the new mode capabilities defined. If it is determined that the receivers 150 or 310 can only understand the legacy mode protocol, then the legacy mode will be used at operation 420. If it is determined that some devices located on the transmitter can use the new mode, the rest of the devices are polled at operation 430 determine if they all can do so. If not, control is passed to operation 420 and the legacy mode is used. Conversely, if all the devices can support the new mode, then the mode of operation at the receiver will be switched at operation 440 and the new mode will then be used via operation 450.

FIG. 3B illustrates a flow diagram for a “set and test” process 460 in accordance with the present invention. The set and test process 460 is another example of how logic 160 and logic 320 function. At an operation 470, the new mode of communication is set. At operation 480, the receiver/interface is tested to see if the new mode is understandable. If the test fails, the old mode of communication is used via operation 490. If the test succeeds, the new mode will be used for communications via operation 500.

FIG. 3C illustrates a flow diagram for a “snoop and test” process 510 in accordance with the present invention. The snoop and test process 510 is yet another example of how logics 160 and 320 can function. At operation 520, the default protocol is used. At an operation 530, the bus is monitored for a response in any format other than the default protocols. Once a transmission is received, it is determined if it differs from the default protocols, at operation 540. If a different protocol is not detected at operation 540, then the transmission will continue to be monitored via operation 530. If a different protocol is detected, then it is decided if the different protocol is recognizable at operation 550. If it isn’t, then the transmission will continue to be monitored via operation 530. If it is recognized, then the new protocol will be used via operation 560.

FIG. 4 illustrates a translator 220 in accordance with the present invention. Translator 220 is also a mirror image of translator 230. SDA (serial data line) and SCL (serial clock line) are the two components of the I²C bus that are connected to the I²C port 580 where SDA and SCL are converted into internal blocks of data. The data is then translated at the translation logic block 590 and connected to the DDC wires 600 via the PHY (physical interface) 610. Some examples of translation logic are ethernet, TCP/IP, current loop, differential signaling and cryptographic encryption/decryption logic.

FIG. 5 illustrates an implementation of a buffer for one line of an I²C bus 100 in accordance with the present invention. Two of these circuits are needed to fully buffer an I²C bus—one for SCL and one for SDA. Buffer 100 is a mirror image of buffer 110. The buffer functions in a way such that data can flow in either direction simultaneously. In order to control the flow of data, a switch is usually necessary but can be difficult to implement. Another way of doing this is to sense the direction a current is flowing and then help it flow in the correct direction. FIG. 5 achieves this function. When a signal at 630 is flowing left to right, node 630 is pulled towards a zero voltage. A positive voltage will then result across the resistor 640 which will in turn be sensed by operational amplifiers 650 and 660. Operational

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amplifier 650 leaves its output transistors 670 in an off-state and operational amplifier 660 turns on its output transistors which in turn brings a signal at 690 down to about a zero voltage as well. If a signal was flowing right to left, an opposite process will occur.

FIG. 6 illustrates a legacy mode of operation in relation to the receiver in accordance with the present invention. The receiver 700 does not have a buffer 100 or a translator 220 as shown on the transmitter 140. In this situation, the switch 120 is kept connected to the buffer 100 by the logic 160, as the receiver can not support the new style protocols. Selection of a firewall 240 on the transmitter 140 is still possible, however.

FIG. 7 illustrates a legacy mode of operation in relation to the transmitter in accordance with the present invention. The transmitter 760 does not have a buffer 110 or a translator 230 as shown on the receiver 150. In this situation, the switch 130 is kept connected to the buffer 110 as defined in the default mode.

The present invention provides a method and apparatus for a two-wire serial command bus interface. The re-mapping allows for high-speed data transmission, data security and is not constrained by length issues. Additionally, a transmitter-side firewall prevents unauthorized access.

An advantage of the present invention is that it is fully compatible with legacy hardware. It intelligently detects whether a device can support new or old protocols and adjusts accordingly. Additionally, even in the absence of new protocol compatibility, it improves upon legacy systems by increasing available cable length and also by providing a transmitter-side firewall.

While this invention has been described in terms certain preferred embodiments, it will be appreciated by those skilled in the art that certain modifications, permutations and equivalents thereof are within the inventive scope of the present invention. It is therefore intended that the following appended claims include all such modifications, permutations and equivalents as fall within the true spirit and scope of the present invention.

What is claimed is:

1. A method for bi-directional transmission of data between a source and a sink over a two-wire interface comprising:

re-mapping a data signal and a clock signal from a first local bus on the source into a different protocol signal; transmitting the different protocol signal from the source to the sink over the two-wire interface;

re-mapping the different protocol signal back into the data signal and the clock signal for use on a second local bus on the sink;

re-mapping the data signal and the clock signal from the second local bus into the different protocol signal; and transmitting the different protocol signal from the sink to the source over the two-wire interface.

2. The method as recited in claim 1 wherein the sink initiates transmission of data to the source.

3. The method as recited in claim 1 or 2 further comprising a logic that determines if the source and the sink are capable of re-mapping the different protocol signal into the data signal and the clock signal.

4. The method as recited in claim 3 wherein the logic directs the source to transmit the data signal and the clock signal over the two-wire interface if the sink is incapable of re-mapping the different protocol signal into the data signal and the clock signal.

5. The method as recited in claim 3 wherein the logic directs the sink to transmit the data signal and the clock

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signal over the two-wire interface if the source is incapable of re-mapping the different protocol signal into the data signal and the clock signal.

6. The method as recited in claim 3 wherein the logic directs the source to transmit the different protocol signal over the two-wire interface if the sink is capable of re-mapping the different protocol signal into the data signal and the clock signal.

7. The method as recited in claim 3 wherein the logic directs the sink to transmit the different protocol signal over the two-wire interface if the source is capable of re-mapping the different protocol signal into the data signal and the clock signal.

8. The method as recited in claim 3 further comprising a set of control registers located on the sink wherein the set of control registers define a list of devices and an associated list of capabilities.

9. The method as recited in claim 8 wherein the logic determines if the sink is capable of re-mapping the different protocol signal into the data signal and the clock signal by:

- directing the source to transmit the data signal and the clock signal over the two-wire interface to the sink;
- soliciting the set of control registers for the list of devices and the associated list of capabilities; and
- directing the source to transmit the different protocol signal if every device from the list of devices is capable of re-mapping the different protocol signal.

10. The method as recited in claim 9 wherein the logic directs the source to transmit the data signal and the clock signal if at least one device from the list of devices is incapable of re-mapping the different protocol signal.

11. The method as recited in claim 8 wherein the logic determines if the source is capable of re-mapping the different protocol signal into the data signal and the clock signal by:

- directing the sink to transmit the data signal and the clock signal over the two-wire interface to the source;
- soliciting the set of control registers for the list of devices and the associated list of capabilities; and
- directing the sink to transmit the different protocol signal if every device from the list of devices is capable of re-mapping the different protocol signal.

12. The method as recited in claim 11 wherein the logic directs the sink to transmit the data signal and the clock signal if at least one device from the list of devices is incapable of re-mapping the different protocol signal.

13. The method as recited in claim 3 wherein the logic determines if the sink is capable of processing the second format data signal and the second format clock signal by:

- directing the source to transmit the different protocol signal over the two-wire interface to the sink; and
- directing the source to continue transmitting the different protocol signal if the sink transmits the different protocol signal over the two-wire interface back to the source.

14. The method as recited in claim 13 wherein the logic directs the source to transmit the data signal and the clock signal if the sink does not transmit the different protocol signal over the two-wire interface back to the source.

15. The method as recited in claim 3 wherein the logic determines if the source is capable of processing the second format data signal and the second format clock signal by:

- directing the sink to transmit the different protocol signal over the two-wire interface to the source; and

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directing the sink to continue transmitting the different protocol signal if the source transmits the different protocol signal over the two-wire interface back to the sink.

16. The method as recited in claim 15 wherein the logic directs the sink to transmit the data signal and the clock signal if the source does not transmit the different protocol signal over the two-wire interface back to the sink.

17. The method as recited in claim 2 further comprising a logic that adaptively determines a type of different protocol signal that the sink is capable of processing.

18. The method as recited in claim 17 wherein the logic adaptively determines the type of different protocol signal by:

- directing the source to transmit a default protocol signal over the two-wire interface to the sink;
- monitoring a two-wire interface for a responding protocol signal;
- receiving the responding protocol signal over the two-wire interface from the sink;
- determining if the default protocol signal and the responding protocol signal differs; and
- directing the source to transmit the responding protocol signal over the two-wire interface to the sink if the default protocol signal and the responding protocol signal differ and if the logic recognizes the responding protocol signal.

19. The method as recited in claim 18 wherein the logic directs the source to transmit the default protocol signal if the default protocol signal and the responding protocol signal do not differ.

20. The method as recited in claim 18 wherein the logic monitors for a response from the sink if the default protocol signal and the responding protocol signal differs and if the logic does not recognize the responding protocol signal.

21. The method as recited in claim 2 further comprising a logic that adaptively determines a type of different protocol signal that the source is capable of processing.

22. The method as recited in claim 21 wherein the logic adaptively determines the type of different protocol signal by:

- directing the sink to transmit a default protocol signal over the two-wire interface to the source;
- monitoring a two-wire interface for a responding protocol signal;
- receiving the responding protocol signal over the two-wire interface from the source;
- determining if the default protocol signal and the responding protocol signal differs; and
- directing the sink to transmit the responding protocol signal over the two-wire interface to the source if the default protocol signal and the responding protocol signal differ and if the logic recognizes the responding protocol signal.

23. The method as recited in claim 22 wherein the logic directs the sink to transmit the default protocol signal if the default protocol signal and the responding protocol signal do not differ.

24. The method as recited in claim 22 wherein the logic monitors for a response from the source if the default protocol signal and the responding protocol signal differs and if the logic does not recognize the responding protocol signal.

25. The method as recited in claim 2 wherein the logic performs a firewall function by closing access to the two-wire interface.

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26. The method as recited in claim 2 wherein the source and the sink both further comprise a buffer.

27. The method as recited in claim 26 wherein the logic performs a firewall function by closing access to the two-wire interface.

28. The method as recited in claim 1 wherein the source is a computer and the sink is a monitor.

29. The method as recited in claim 1 wherein the source is a video source and the sink is a monitor.

30. The method as recited in claim 29 wherein the video source is a DVD player.

31. The method as recited in claim 29 wherein the video source is a video cassette recorder.

32. The method as recited in claims 28, 29, 30 or 31 wherein the monitor is a television.

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33. The method as recited in claim 1 wherein the different protocol signal is defined in an ethernet protocol.

34. The method as recited in claim 1 wherein the different protocol signal is defined in a TCP/IP protocol.

35. The method as recited in claim 1 wherein the different protocol signal is defined in an RS-232 protocol.

36. The method as recited in claim 1 wherein the different protocol signal is defined in a current loop protocol.

37. The method as recited in claims 1 or 2 wherein the data signal, the clock signal and the different protocol signal are transmitted over the two-wire interface simultaneously.

* * * * *